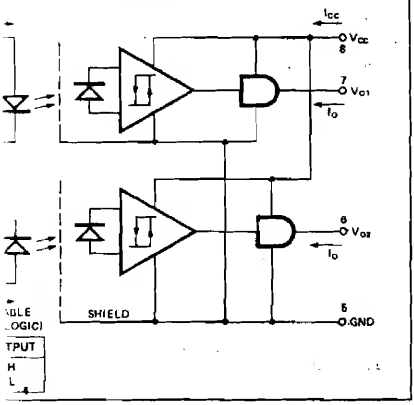
HEWLETT PACKARD

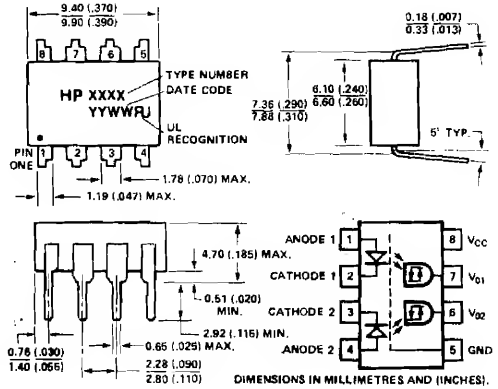
VERY HIGH CMR, WIDE V_{CC} DUAL LOGIC GATE OPTOCOUPLER

HCPL-2231
HCPL-2232

SCHEMATIC



OUTLINE DRAWING



DIMENSIONS IN MILLIMETRES AND (INCHES).

res

IGH COMMON MODE REJECTION 10 kV/μs
V GUARANTEED (HCPL-2232)
CC RANGE (4.5 TO 20 VOLTS)
ROPAGATION DELAY GUARANTEED
HE FULL TEMPERATURE RANGE
YPICAL SIGNAL RATE
PUT CURRENT (1.8 mA)
POLE OUTPUT (NO PULLUP
OR REQUIRED)
NTEED PERFORMANCE FROM
O +85°C
NIZED UNDER THE COMPONENT
AM OF U.L. (FILE NO. E55361) FOR
TRIC WITHSTAND PROOF TEST
ES OF 2500 Vac, 1 MINUTE
ROVED
D-1772 VERSION AVAILABLE
5230/1)

tions

ON OF HIGH SPEED LOGIC SYSTEMS
TER-PERIPHERAL INTERFACES
ROCESSOR SYSTEM INTERFACES
D LOOP ELIMINATION
TRANSFORMER REPLACEMENT
EED LINE RECEIVER

Description

The HCPL-2231/2 are dual-channel, optically-coupled logic gates. The detectors have totem pole output stages and optical receiver input stages with built-in Schmitt triggers to provide logic compatible waveforms, eliminating the need for additional waveshaping.

A superior internal shield on the HCPL-2232 guarantees common mode transient immunity of 10,000 V/μs at a common mode voltage of 1000 V_{CM}.

The electrical and switching characteristics of the HCPL-2231/2 are guaranteed from -40°C to +85°C and a V_{CC} from 4.5 volts to 20 volts. Low I_F and wide V_{CC} range allow compatibility with TTL, LSTTL, and CMOS logic and result in lower power consumption compared to other high speed couplers. Logic signals are transmitted with a typical propagation delay of 150 ns.

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	V_{CC}	4.5	20	Volts
Input Current (High)	$I_{F(ON)}$	1.8*	5	mA
Input Voltage (Low)	$V_{F(OFF)}$	—	0.8	Volts
Operating Temperature	T_A	-40	85	°C
Fan Out per Channel	N		4	TTL Loads

*The initial switching threshold is 1.8 mA or less. It is recommended that 2.5 mA be used to permit at least a 20% CTR degradation guardband.

OPTO COUPLERS

Recommended Circuit Design

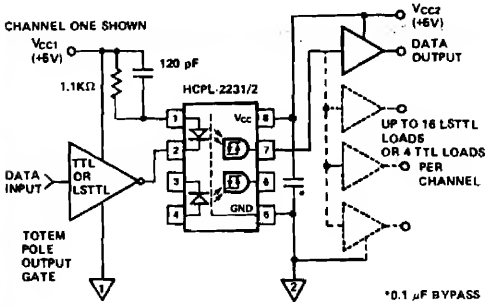


Figure 1. Recommended LSTTL to LSTTL Circuit

Absolute Maximum Ratings

Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... −40°C to +85°C
Lead Solder Temperature ..... 260°C for 10 s
(1.6 mm below seating plane)
Average Forward Input Current — I_F ..... 10 mA[1]
Peak Transient Input Current — I_F ..... 1 A[1]
(≤1 μs Pulse Width, 300 pps)
Reverse Input Voltage ..... 5 V[1]
Supply Voltage — V_{CC} ..... 0.0 V min., 20 V max.
Output Voltage — V_O ..... −0.5 V min., 20 V max.[1]
Total Package Power Dissipation ..... 294 mW
Output Power Dissipation — P_O per Channel ..... Fig. 8
Average Output Current — I_O per Channel ..... 25 mA

Electrical Specifications

$-40°C \le T_A \le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.8\ mA \le I_{F(ON)} \le 5\ mA$, $0\ V \le V_{F(OFF)} \le 0.8\ V$, unless otherwise specified.
All Typicals at $T_A = 25°C$. See note 7.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions		Figure	Note
Logic Low Output Voltage	V_{OL}			0.5	Volts	I_{OL} = 6.4 mA (4 TTL Loads)		2, 4	1
Logic High Output Voltage	V_{OH}	2.4 2.7			Volts	I_{OH} = −2.6 mA I_{OH} = −0.4 mA	V_{CC} = 4.5 V	3, 4, 9	1
Output Leakage Current ($V_{OUT} > V_{CC}$)	I_{OHH}			100	μA	V_O = 5.5 V	I_F = 5 mA V_{CC} = 4.5 V		1
				500	μA	V_O = 20 V			
Logic Low Supply Current	I_{CCL}		7.4	12.0	mA	V_{CC} = 5.5 V	V_F = 0 V I_O = Open		
			8.6	14.0	mA	V_{CC} = 20 V			
Logic High Supply Current	I_{CCH}		4.8	8.0	mA	V_{CC} = 5.5 V	I_F = 5 mA		
			5.4	10.0	mA	V_{CC} = 20 V			
Logic Low Short Circuit Output Current	I_{OSL}	15			mA	$V_O = V_{CC}$ = 5.5 V	V_F = 0 V I_O = Open		1, 2
		20			mA	$V_O = V_{CC}$ = 20 V			
Logic High Short Circuit Output Current	I_{OSH}	−10			mA	V_{CC} = 5.5 V	I_F = 5 mA V_O = GND		1, 2
		−20			mA	V_{CC} = 20 V			
Input Forward Voltage	V_F		1.5	1.7 1.85	Volts	T_A = 25°C	I_F = 5 mA	5	1
Input Reverse Breakdown Voltage	BV_R	5			Volts	I_R = 10 μA			1
Input Diode Temperature Coefficient	$\frac{\Delta V_F}{\Delta T_A}$		−1.7		mV/°C	I_F = 5 mA			
Input-Output Insulation	V_{ISO}	2500			V_{RMS}	RH ≤ 50%, t = 1 min., T_A = 25°C			3, 8
Input-Output Resistance	R_{I-O}		10^{12}		ohms	V_{I-O} = 500 VDC			3
Input-Output Capacitance	C_{I-O}		0.6		pF	f = 1 MHz, V_{I-O} = 0 VDC			3
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V			1
Input-Input Insulation Leakage Current	I_{I-I}		0.005		μA	Relative Humidity = 45% t = 5 s, V_{I-I} = 500 V			6
Resistance (Input-Input)	R_{I-I}		10^{11}		Ω	V_{I-I} = 500 V			6
Capacitance (Input-Input)	C_{I-I}		0.25		pF	f = 1 MHz			6

Switching Specifications $-40°C \le T_A \le 85°C$, $4.5\ V \le V_{CC} \le 20\ V$, $1.8\ mA \le I_{F\ (ON)} \le 5\ mA$, $0\ V \le V_{F\ (OFF)} \le 0.8\ V$. All Typicals at $T_A = 25°C$, $V_{CC} = 5\ V$, $I_{F\ (ON)} = 3\ mA$ unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions	Figure	Note
Propagation Delay Time to Logic Low Output Level	t_{PHL}		150		ns	Without Peaking Capacitor	6, 7	1, 4
			150	300		With Peaking Capacitor		
Propagation Delay Time to Logic High Output Level	t_{PLH}		110		ns	Without Peaking Capacitor	6, 7	1, 4
			90	300		With Peaking Capacitor		
Output Rise Time (10–90%)	t_r		30		ns		6, 10	1
Output Fall Time (90–10%)	t_f		7		ns		6, 10	1

Parameter	Symbol	Device	Min.	Units	Test Conditions		Figure	Note
Logic High Common Mode Transient Immunity	$\|CM_H\|$	HCPL-2231	1,000	V/μs	$\|Vcm\| = 50\ V$	$I_F = 1.8\ mA$, $V_{CC} = 5\ V$, $T_A = 25°C$	11	1, 5
		HCPL-2232	10,000	V/μs	$\|Vcm\| = 1{,}000\ V$			
Logic Low Common Mode Transient Immunity	$\|CM_L\|$	HCPL-2231	1,000	V/μs	$\|Vcm\| = 50\ V$	$V_F = 0\ V$, $V_{CC} = 5\ V$, $T_A = 25°C$	11	1, 5
		HCPL-2232	10,000	V/μs	$\|Vcm\| = 1{,}000\ V$			

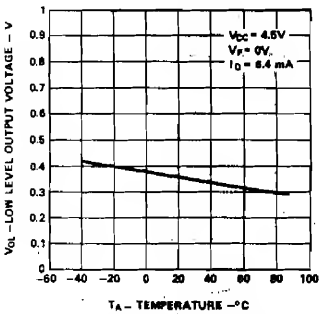


Figure 2. Typical Logic Low Output Voltage vs. Temperature

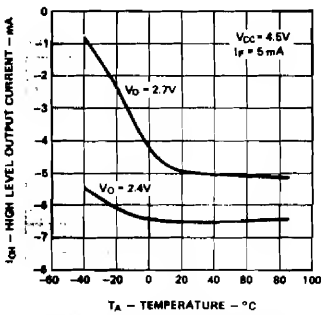


Figure 3. Typical Logic High Output Current vs. Temperature

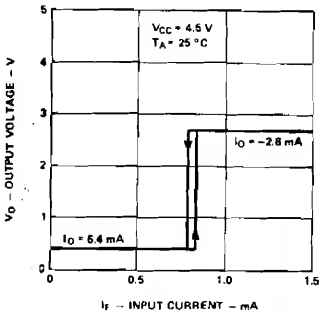


Figure 4. Output Voltage vs. Forward Input Current

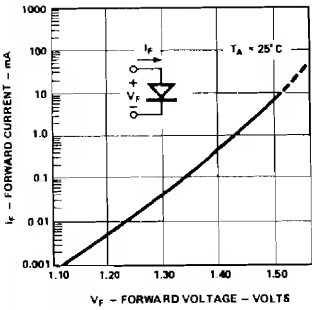
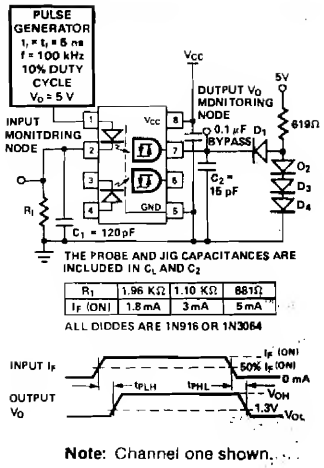


Figure 5. Typical Input Diode Forward Characteristic



Note: Channel one shown.

Figure 6. Circuit for t_{PLH}, t_{PHL}, t_r, t_f

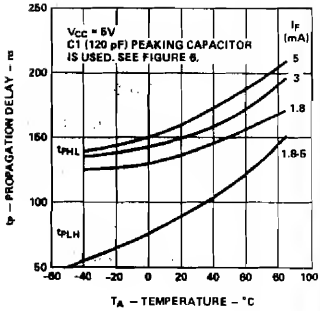


Figure 7. Typical Propagation Delays vs. Temperature

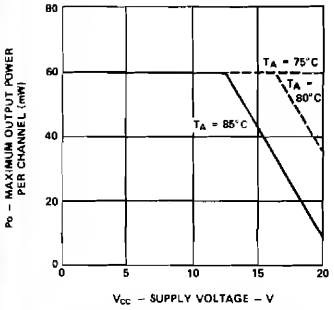


Figure 8. Maximum Output Power per Channel vs. Supply Voltage

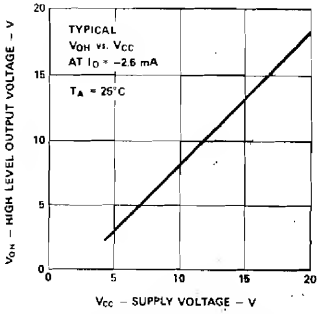


Figure 9. Typical Logic High Output Voltage vs. Supply Voltage

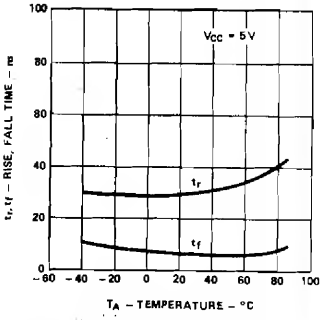


Figure 10. Typical Rise, Fall Time vs. Temperature

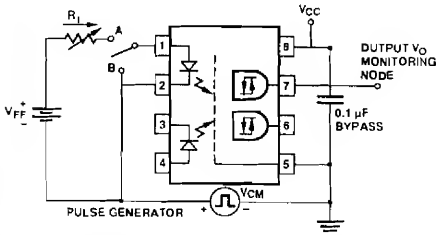


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

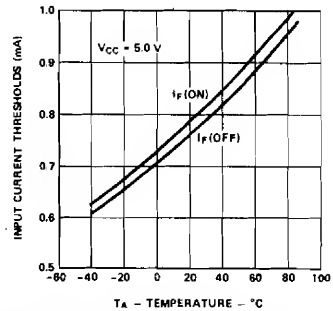


Figure 12. Typical Input Threshold Current vs. Temperature

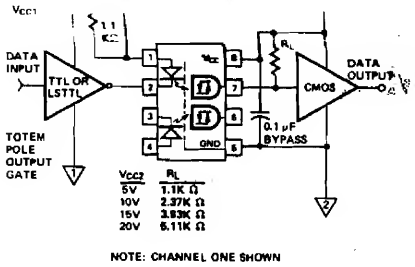


Figure 13. LSTTL to CMOS Interface Circuit

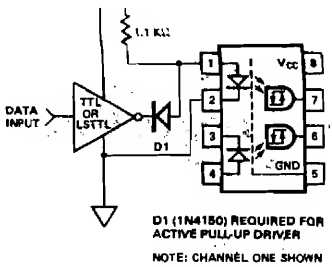


Figure 14. Alternate LED Drive Circuit

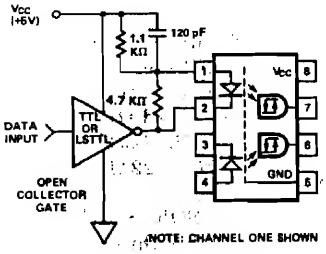


Figure 15. Series LED Drive with Open Collector Gate (4.7 kΩ Resistor Shunts I_{OH} from the LED)

Notes:

1. Each channel.
2. Duration of output short circuit time should not exceed 10 ms.
3. Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
4. The t_{PLH} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.3 V point on the leading edge of the output pulse. The t_{PHL} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.3 V point on the trailing edge of the output pulse.
5. CM_L is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic low state. $V_O < 0.8$ V. CM_H is the maximum slew rate of the common mode voltage that can be sustained with the output voltage in the logic high state $V_O > 2.0$ V.
6. Measured between pins 1 and 2, shorted together, and pins 3 and 4, shorted together.
7. Use of a 0.1 μF bypass capacitor connected between pins 5 and 8 is recommended.
8. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{rms} for 1 second (leakage detection current limit, $I_{i-o} \leq 5$ μA)